

Vidyasagar Sir's Simple Notes, BSc I Year, Sem-2 Digital Electronics www.vsa.edu.in

### 1.9 INTRODUCTION

A logic circuit is so named, because it can simulate human mental process like to take decisions. It is a combination of different electronic components, which obeys laws of Boolean algebra and digital electronics.

Thus, it produces required result at its output. Logic high or logic-1 means a state in digital circuit, when its input/output is positive or above ground level (i.e. in I quadrant, above x-axis). This state is indicated by a ' 1 '.

Similarly, logic low or logic-0 means a state in digital circuit, when its input/output is negative (i.e. at ground level or below ground level). This logic state of the circuit is indicated by a ' 0 '. But the inverse of binary state is also produced by some logic circuits. For example, if input is 1 , then the output will be 0 and vice versa. This process is called the inversion of binary state is called complement of a bit.

### 1.10 BASIC GATES

There are three types of basic gates. They are AND gate, OR gate and NOT gate. These are also known as logic circuits because they can perform different logical functions.

### 1.10.1 AND LOGIC GATE

Definition: An AND gate is a logic circuit, whose output becomes high ONLY WHEN ALL ITS INPUTS ARE HIGH. Its logic equation is $Y=A . B$.

This equation shows that inputs A \& B are related to each other with AND mathematical operator. Thus, when A AND B both are high, then only Y is high, otherwise low. In this way. AND multiplication rules for all possible inputs combinations are -

When $\mathrm{A}=\mathrm{B}=0$, then $\mathrm{Y}=\mathrm{A} \cdot \mathrm{B}=0.0=0$
When $A=0, B=1$, then $Y=A \cdot B=0.1=0$
When $A=1, B=0$, then $Y=A \cdot B=1.0=0$
When $A=B=1$, then only $Y=A . B=1.1=1$


| $\mathbf{A}$ | $\mathbf{B}$ | $\mathbf{Y}=\mathbf{A}+\mathbf{B}$ |
| :---: | :---: | :---: |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

### 1.10.2 OR LOGIC GATE

Definition: An OR gate is a logic circuit whose output becomes high WHEN ANY ONE OF ITS INPUTS IS HIGH. Its logic equation is $Y=A+B$. It is also called inclusive OR gate.

This equation shows that inputs A and B are related with OR mathematical operator. Thus, when A OR $B$ is high, $Y$ is high. The OR addition rules for all possible combinations of inputs are -

When $A=B=0, Y=A+B=0+0=0$
When $\mathrm{A}=0, \mathrm{~B}=1, \mathrm{Y}=\mathrm{A}+\mathrm{B}=0+1=1$
When $\mathrm{A}=1, \mathrm{~B}=0, Y=\mathrm{A}+\mathrm{B}=1+0=1$
When $A=B=1, Y=A+B=1+1=1$


| $\mathbf{A}$ | $\mathbf{B}$ | $\mathbf{Y}=\mathbf{A}+\mathbf{B}$ |
| :---: | :---: | :---: |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

### 1.10.3 NOT LOGIC GATE

Definition: A NOT gate has only one input and one output. It gives high output WHEN ITS INPUT IS LOW. Its logic equation is $Y=\bar{A}$. Thus, it shows that Y is complement of A. The rules of NOT operations are -

When $\mathrm{A}=0$, then $\mathrm{A}=\overline{0}=1$
When $\mathrm{A}=1$, then $\mathrm{A}=\overline{1}=0$


| $\mathbf{A}$ | $\boldsymbol{Y}=\overline{\boldsymbol{A}}$ |
| :---: | :---: |
| 0 | 1 |
| 1 | 0 |

### 1.11 BOOLEAN ALGEBRA

When we deal with logic, we actually face with two-valued question. Its answer will be either in YES or NO! The English mathematician George Boole assigned two symbols to the solutions: Yes $=\mathbf{1}$ and $\mathbf{N o}=\mathbf{0}$. This is called method of reasoning to answer a two-valued question. Thus, the Boolean algebra is mainly used in digital circuits to manipulate, design and analyze the working of electronic circuits in terms of high or low, 1 or 0 , yes or no, true or false etc.

### 1.11.1 LAWS OF BOOLEAN ALGEBRA

According to Boolean algebra, A, B, C... are the variables which can take two possible values. They can be either a 1 or a 0 . The laws are as follows -

## Law of commutativity

$$
\begin{aligned}
& A+B=B+A \\
& A . B=B \cdot A
\end{aligned}
$$

## Law of associativity

$$
\begin{aligned}
& A+(B+C)=(A+B)+C \\
& A \cdot(B \cdot C)=(A \cdot B) \cdot C
\end{aligned}
$$

## Distributive Law

$$
A \cdot(B+C)=A \cdot B+B \cdot C
$$

### 1.11.2 BASIC RULES OF BOOLEAN ALGEBRA

## Rules of addition

$$
0+0=0, \quad 0+1=1, \quad 1+0=1, \quad 1+1=1
$$

## Rules of multiplication

$$
0 \cdot 0=0, \quad 0.1=0, \quad 1 \cdot 0=0, \quad 1 \cdot 1=1
$$

These rules should be remembered in order to solve different problems on logic circuits. They are useful to reduce the complicated logical equations into simple form. Above rules are also applicable to the variables like A, B, C. Thus, we can have -

$$
A+A=A \quad \text { and } \quad A \cdot A=A
$$

## Exercise on the Topic

1. Draw the symbol of AND logic circuit and explain it will its truth table and its symbol.
2. How an OR gate logic circuit works? Explain its working with the help of truth table and symbol.
3. Why the output condition of NOT logic circuit is opposite to its input? Draw the symbol of NOT gate and explain its working with truth table.
4. If $\mathrm{A}+\mathrm{A}=\mathrm{A}$, then $\mathrm{AB}+\mathrm{AB}=$ ? By putting the values of the variables as 1 or 0 in the given equation and obtain the result.
5. If $\mathrm{A} \cdot(\mathrm{B}+\mathrm{C})=\mathrm{AB}+\mathrm{AC}$, then calculate the result of $\mathrm{AB} \cdot(\mathrm{A}+\mathrm{B})=$ ?
6. If $A+A=A$ and $A . A=A$, then is it true that $A+A=A . A$ ? By putting the values of the variables as 1 or 0 in the given equation check the result.

### 1.12 PROOFS OF BOOLEAN ALGEBRA

There are some important proofs used in Boolean algebra. The student must prepare all these proofs to solve complicated logic equations effectively. In the following proofs we have to prove that for given statement LHS = RHS. Also to prove these equations, we shall consider that the variables take two possible values either 1 or 0 .

1. $A+1=1$
2. $A+A=A$
3. $A .1=A$
4. $\bar{A}+A=1$
5. $\bar{A} \cdot A=0$
6. $A . A=A$
7. $\overline{\bar{A}}=A$
8. $A+A B=A$

## Exercise on the Topic

1. If $A+A B=A$, then calculate the output of $A+A B+A C B=$ ?
2. If $\bar{A}=0$, then $A=$ ?
3. According to the basic proofs, if $A+1=A$, then $\bar{A} . B+1=$ ?
4. Suppose $\bar{A}=1$ and $\bar{A}$. $B=0$, then $B=$ ?
5. Calculate the output result of the equation $A+A B+C A+B C=$ ?
6. If $\bar{A}+A=1$, then calculate $\overline{A B}+A B=$ ?
7. $\bar{A} \cdot A=0$, then calculate the output result of $\overline{A B} \cdot A B=$ ?
8. $A C+A B+A B C+A C D B+A B C D E A=$ ?
9. $C \bar{A}+\bar{A} B C+B C+A=$ ?
10. $\bar{A} \cdot 1+A+1=$ ?
11. $\bar{A} \cdot A+1=$ ?
12. $\bar{A} \cdot(B+C+A B)=$ ?
13. $A \cdot(\bar{A}+A)=$ ?

### 1.13 DE MORGAN'S THEOREMS

It is an important tool in solving the complicated logical equations while analyzing the logical circuits. There are two theorems of De Morgan. They are known as theorem \#1 and theorem \#2. The sequence of these theorems may change, but the basic idea of both the theorems remains the same.

### 1.13.1 FIRST THEOREM

Definition: It states that the complement of product is equal to the sum of the complements.
Special case: $\overline{A .} \bar{B}=\bar{A}+\bar{B}$, General case: $\overline{A . B . C \ldots}=\bar{A}+\bar{B}+\bar{C} \ldots$
Proof: We shall prove above theorem by showing that LHS \& RHS of given equation are equal.
Suppose, $L H S=\overline{A B}$
Let $\mathrm{A}=\mathrm{B}=0$, then $\overline{\mathrm{AB}}=\overline{0.0}=\overline{0}=1$
Let $A=0, B=1$, then $\overline{\mathrm{AB}}=\overline{0.1}=\overline{0}=1$
Let $\mathrm{A}=1, \mathrm{~B}=0$, then $\overline{\mathrm{AB}}=\overline{1.0}=\overline{0}=1$
Let $\mathrm{A}=1, \mathrm{~B}=1$, then $\overline{\mathrm{AB}}=\overline{1.1}=\overline{1}=0$

| A | B | LHS | RHS |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 |

Suppose, $R H S=\bar{A}+\bar{B}$
Let $\mathrm{A}=\mathrm{B}=0$, then $\overline{\mathrm{A}}+\overline{\mathrm{B}}=\overline{0}+\overline{0}=1+1=1$
Let $\mathrm{A}=0, \mathrm{~B}=1$, then $\overline{\mathrm{A}}+\overline{\mathrm{B}}=\overline{0}+\overline{1}=1+0=1$


Let $\mathrm{A}=1, \mathrm{~B}=0$, then $\overline{\mathrm{A}}+\overline{\mathrm{B}}=\overline{1}+\overline{0}=0+1=1$
Let $\mathrm{A}=1, \mathrm{~B}=1$, then $\overline{\mathrm{A}}+\overline{\mathrm{B}}=\overline{1}+\overline{1}=0+0=0$


### 1.13.2 SECOND THEOREM

Definition: It states that the complement of sum is equal to the product of the complements.

$$
\text { Special case: } \overline{A+B}=\bar{A} \cdot \bar{B}, \text { General case: } \overline{A+B+C \ldots}=\bar{A} \cdot \bar{B} \cdot \bar{C} \ldots
$$

Proof: We shall prove above theorem by showing that LHS \& RHS of given equation are equal.
Suppose, $L H S=\overline{A+B}$
Let $A=B=0$, then $\overline{A+B}=\overline{0+\overline{0}}=\overline{0}=1$
Let $A=0, B=1$, then $\overline{A+B}=\overline{0+1}=\overline{1}=0$
Let $A=1, B=0$, then $\overline{A+B}=\overline{1+0}=\overline{1}=0$
Let $A=1, B=1$, then $\overline{A+B}=\overline{1+1}=\overline{1}=0$

| A | B | LHS | RHS |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 |

Suppose, $R H S=\bar{A} \cdot \bar{B}$
Let $A=B=0$, then $\bar{A} \cdot \bar{B}=\overline{0} \cdot \overline{0}=1.1=1$


Let $A=0, B=1$, then $\bar{A} \cdot \bar{B}=\overline{0} \cdot \overline{1}=1.0=0$
Let $A=1, B=0$, then $\bar{A} \cdot \bar{B}=\overline{1} \cdot \overline{0}=0.1=0$
Let $A=1, B=1$, then $\bar{A} \cdot \bar{B}=\overline{1} \cdot \overline{1}=0.0=0$


## Exercise on the Topic

1. Calculate the output result of the logic equation: $Y=A+\overline{A . B}$
2. If $Y=(\bar{A}+\bar{B}) \cdot(\bar{A}+B) \cdot(A+\bar{B})$, then calculate the value of $Y$.
3. $Y=(\overline{A B})+(\overline{B C})+(\overline{A C})$, then calculate the value of $Y$.
4. What is the output result of the equation: $Y=(\bar{A}+\bar{B}) .(A+B)$.
5. Calculate the output result of the logic equation: $Y=(\bar{A}+B+C) \cdot(A+\bar{B}+C) \cdot(A+B+\bar{C})$.

### 1.14 DERIVED GATES

When basic gates are connected in different combination, a new type of gate is produced known as derived gate. Basically there are two types of derived gates known as NAND gate and NOR gate.

### 1.14.1 NAND GATE

Definition: A NAND gate is a logic circuit, whose output becomes low only when all its inputs are high. In other words, its output is high when at least one of its inputs is low. Its output equation, truth table and the proof of logical conditions are given below. Since it is produced by combining NOT gate and AND gate, the circuit is called NOT-AND gate, i.e. NAND gate.

$$
Y=\overline{A \cdot B}
$$

Let $\mathrm{A}=\mathrm{B}=0$, then $\overline{\mathrm{AB}}=\overline{0.0}=\overline{0}=1$
Let $A=0, B=1$, then $\overline{\mathrm{AB}}=\overline{0.1}=\overline{0}=1$
Let $\mathrm{A}=1, \mathrm{~B}=0$, then $\overline{\mathrm{AB}}=\overline{1.0}=\overline{0}=1$
Let $\mathrm{A}=1, \mathrm{~B}=1$, then $\overline{\mathrm{AB}}=\overline{1.1}=\overline{1}=0$

| $\mathbf{A}$ | $\mathbf{B}$ | $\boldsymbol{Y}=\overline{\boldsymbol{A} . \boldsymbol{B}}$ |
| :---: | :---: | :---: |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |



### 1.14.2 NOR GATE

Definition: A NOR gate is a logic circuit whose output becomes low when any one of its inputs is low. In other words, i.e. its output becomes high when both of its inputs are low. Its output equation, truth table and the proof of logical conditions are given below. Since it is produced by combining NOT gate and OR gate, the circuit is called NOT- OR gate, i.e. NOR gate.

$$
Y=\overline{A+B}
$$

Let $A=B=0$, then $\overline{A+B}=\overline{0+0}=\overline{0}=1$
Let $A=0, B=1$, then $\overline{A+B}=\overline{0+1}=\overline{1}=0$
Let $A=1, B=0$, then $\overline{A+B}=\overline{1+0}=\overline{1}=0$
Let $A=1, B=1$, then $\overline{A+B}=\overline{1+1}=\overline{1}=0$

| $\mathbf{A}$ | $\mathbf{B}$ | $\boldsymbol{Y}=\overline{\boldsymbol{A + B}}$ |
| :---: | :---: | :---: |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |



## Exercise on the Topic

1. Calculate the value of output $Y$, of the following logic circuits if inputs are $A$ and $B$.


2. What is the output $Y$, of the following logic circuits if inputs are $A$ and $B$.

3. What will happen if the output of one NOT gate is connected to the input of the second NOT gate? Explain with diagram and obtain the output logic equation.

### 1.15 UNIVERSAL BUILDING BLOCKS

The above logic circuits NAND gate and NOR gate are called universal building blocks, because using these logic circuits, we can construct any type of logic circuit i.e. AND, OR, NOT, NAND or NOR gate. For this, the rules mentioned in Topic \#2.4 and the De Morgan's both theorems are important.

### 1.15.1 NOT GATE USING NAND GATE

When both inputs of a NAND gate are connected to each other and treated as single input it forms a
 NOT gate. Here both input terminals of NAND gate are connected together. So input signal at terminal A will be equally distributed to both inputs of NAND gate. Hence, the output will be the same as NOT gate with a single input. Thus, any NAND gate with any number inputs can be converted into equivalent NOT gate using this method.

## Mathematical analysis of the logic circuit:

$$
\begin{array}{lll}
\text { When } A=0, Y=\overline{0.0}=\overline{0}=1=\bar{A} & \text { i.e. } & Y=\bar{A} \\
\text { When } A=1, Y=\overline{1.1}=\overline{1}=0=\bar{A} & \text { i.e. } & Y=\bar{A}
\end{array}
$$

### 1.15.2 OR GATE USING NAND GATE

When three NAND gates are connected in the circuit as shown below, an OR gate is formed. In the following circuit, NAND gate 1 and 2 are used as NOT gates and their outputs are connected to the input terminals of NAND gate 3. The mathematical analysis of the circuit is given below -


$$
\begin{aligned}
& Y_{1}=\bar{A}, \quad Y_{2}=\bar{B} \quad \therefore Y=\bar{Y}_{1}+\bar{Y}_{2} \\
& \therefore Y=\bar{A} \bar{A} \cdot \bar{B}=\bar{A}+\bar{B}=A+B
\end{aligned}
$$

Thus, by applying De Morgan's theorem, we obtain the output logical equation of the circuit. So using three NAND gates we can obtain one OR gate. However, this circuit is only experimental idea to understand basic working of NAND gate.

### 1.15.3 AND GATE USING NAND GATE

When two NAND gates are connected one after another, as shown in the following circuit, an AND gate is formed. Here, NAND gate 1 has two input terminals and NAND gate 2 is used as NOT gate. The mathematical analysis of the circuit is given below.


$$
\begin{aligned}
& Y_{1}=\overline{A B} \quad \text { and } \quad Y=\bar{Y}_{1} \\
& \therefore Y=\overline{\overline{A . B}}=A . B
\end{aligned}
$$

Thus, by applying simple Boolean algebra, we obtain the output logical equation of the circuit. So using two NAND gates we can obtain one AND gate. However, this circuit is only experimental idea to understand basic working of NAND gate.

### 1.16 IDENTITIES OF BOOLEAN ALGEBRA

Understanding the logic circuits give us an effective tool in solving complicated logical equations. Following are the identities, in which we have to prove that LHS $=$ RHS.

1. $(\bar{A}+\bar{B}) \cdot(\bar{A}+B) \cdot(A+\bar{B})=A B$
2. $(\bar{A}+B+C) \cdot(A+\bar{B}+C) \cdot(A+B+\bar{C})=A B+B C+A C+\bar{A} \cdot \bar{B} \cdot \bar{C}$
3. $A+\bar{A} \cdot B=A+B$
4. $(A+B) \cdot(A+C)=A+B C$
5. $\overline{A B+B C+C A}=\bar{A} \cdot \bar{B}+\bar{B} \cdot \bar{C}+\bar{C} \cdot \bar{A}$
6. $A B+A C+B \bar{C}=A C+B \bar{C}$
7. $\overline{\bar{A}+B}+\overline{\bar{A}+\bar{B}}=A$
8. $A B+C A B+D B C A+D B A C E=A$
9. $A \cdot(\bar{A}+B)=A B$
10. $\bar{B} \cdot \bar{C}+\bar{D} \cdot \bar{A} \cdot \bar{C}+\bar{D} \cdot A \cdot B \cdot \bar{C}+D \cdot B \cdot \bar{C}=\bar{C}$

### 1.17 EXCLUSIVE OR GATE (EX-OR GATE)

Definition: An Exclusive OR gate is defined as a logic circuit whose output becomes high only when its both inputs are UNEQUAL.

It is a special type of logic circuit used in digital electronics. Its logic equations are -

$$
Y=\bar{A} \cdot B+A \bar{B} \quad Y=A \oplus B
$$

The Ex-OR addition rules for all possible combinations of inputs are given below -
a) When $\mathrm{A}=\mathrm{B}=0, \mathrm{Y}=\overline{\mathrm{A}} \cdot \mathrm{B}+\mathrm{A} \cdot \overline{\mathrm{B}}=0$
$\mathrm{A} \oplus \mathrm{B}=0 \oplus 0=0$
b) When $\mathrm{A}=0, \mathrm{~B}=1, \mathrm{Y}=\overline{\mathrm{A}} \cdot \mathrm{B}+\mathrm{A} \cdot \overline{\mathrm{B}}=1$
$\mathrm{A} \oplus \mathrm{B}=0 \oplus 1=1$
c) When $\mathrm{A}=1, \mathrm{~B}=0, \mathrm{Y}=\overline{\mathrm{A}} \cdot \mathrm{B}+\mathrm{A} \cdot \overline{\mathrm{B}}=1$
$\mathrm{A} \oplus \mathrm{B}=1 \oplus 0=1$
d) When $\mathrm{A}=\mathrm{B}=1, \mathrm{Y}=\overline{\mathrm{A}} \cdot \mathrm{B}+\mathrm{A} \cdot \overline{\mathrm{B}}=0$
$\mathrm{A} \oplus \mathrm{B}=1 \oplus 1=0$

| $\mathbf{A}$ | $\mathbf{B}$ | $\mathbf{Y}=\mathbf{A} \oplus \mathbf{B}$ |
| :---: | :---: | :---: |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |



### 1.17.1 EX-OR GATE USING NAND GATES

When four NAND gates are connected in particular combination as shown in the following circuit, one Ex-OR gate is formed. In this circuit, gate 1 has two inputs A \& B. Its output is connected in parallel to one input terminal of gate 2 and gate 3 . Their other inputs are connected to terminal A \& B. Finally, the outputs of gate 2 and gate 3 are connected to two input terminals of gate 4 . The output of gate 4 is $Y$.

Now $Y_{1}$ is the output of gate 1 , which is given by -

$$
Y_{1}=\overline{A \cdot B}
$$

Now $Y_{2}$ and $Y_{3}$ are the outputs of gate 2 and gate 3 . They are given as -

$$
Y_{2}=\overline{A \cdot Y_{1}}=\overline{A \cdot(\overline{A \cdot B})} \quad \text { and } \quad Y_{3}=\overline{B \cdot Y_{1}}=\overline{B \cdot(\overline{A \cdot B})}
$$



| $\mathbf{A}$ | $\mathbf{B}$ | $\mathbf{Y}=\mathbf{A} \oplus \mathbf{B}$ |
| :---: | :---: | :---: |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Finally, the $Y$ is the output of gate 4 , which is given by -

$$
Y=\overline{Y_{2} \cdot Y_{3}}=\overline{(\overline{A \cdot(\overline{A \cdot B})}) \cdot(\overline{B \cdot(\overline{A \cdot B})})}
$$

Now applying De Morgan's theorem to the equation, $Y=\overline{Y_{2} \cdot Y_{3}}$, we get -

$$
\begin{aligned}
& \therefore Y= \bar{Y}_{2}+\bar{Y}_{3}= \\
&\quad \therefore Y=A \cdot(\overline{(\overline{A \cdot B})+B \cdot(\overline{A \cdot B})})+\overline{(\overline{B \cdot B})} \overline{(\overline{A \cdot B})})
\end{aligned}
$$

Now finally applying De Morgan's theorem to the brackets, we get -

$$
\begin{aligned}
& \therefore Y=A \cdot(\bar{A}+\bar{B})+B \cdot(\bar{A}+\bar{B}) \\
& \therefore Y=A \cdot \bar{A}+A \cdot \bar{B}+B \cdot \bar{B}+\bar{A} \cdot B
\end{aligned}
$$

But according to Boolean algebra, $A \cdot \bar{A}=0$ and $B . \bar{B}=0$. So finally, we get -

$$
Y=A \cdot \bar{B}+\bar{A} \cdot B=Y=A \oplus B
$$

### 1.17.2 EX-OR GATE USING BASIC GATES

When all the basic gates are connected in particular combination as shown below, we get Ex-OR logic
 circuit. The mathematical analysis of the circuit is given below -

$$
Y_{1}=\bar{A} \text { and } Y_{2}=\bar{B}
$$

Similarly, $Y_{3}=\bar{A} . B$ and $Y_{4}=A \cdot \bar{B}$
Now the final output $Y$ will be the output of OR gate, so we get -

$$
Y=Y_{3}+Y_{4}=A . \bar{B}+\bar{A} . B \quad \text { i.e. } \quad Y=A \oplus B
$$

### 1.17.3 PARITY AND PARITY CHECKER

Always remember that parity means a single binary 1 . Thus, if a binary number is given as: $(1101)_{2}$ then it contains three parities. Such binary number is called as odd parity binary "word". But if a binary number is given as: $(1001101)_{2}$ then it contains four parities. Then such number is called even parity binary "word".

The Ex-OR gate is ideal for testing the number of parities present in very large binary word. This logic circuit (gate) can recognize odd number of parities. Thus, odd parity input to the following circuit produces the output as $Y=1$ but when even parity input gives $Y=0$. This is shown in the following circuit -


Here, if $Y=A_{3} A_{2} A_{1}=110$, then the output of the circuit will be -

$$
Y=0
$$

Here, if $Y=A_{3} A_{2} A_{1}=010$, then the output of the circuit will be -

$$
Y=1
$$

### 1.18 HALF ADDER

It is combination of basic logic gates. Using this circuit, we can add two binary digits at a time. In half adder, there are two inputs $A$ and $B$ with two outputs SUM and CARRY. The SUM is the output of ExOR gate and CARRY is the output of AND gate. Remember that SUM is at LSB position and CARRY is at MSB position.


| A | B | Carry | Sum |
| :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

## Mathematical analysis of the logic circuit:

Let $A=B=0$, then $\operatorname{SUM}=0$ and $\operatorname{CARRY}=0$, so the result of addition will be 00 .
Let $A=0, B=1$, then $\operatorname{SUM}=1$ and $\operatorname{CARRY}=0$, so the result of addition will be 01 .
Let $A=1, B=0$, then $\operatorname{SUM}=1$ and $\operatorname{CARRY}=0$, so the result of addition will be 01 .
Let $A=B=1$, then $\operatorname{SUM}=1$ and $\operatorname{CARRY}=0$, so the result of addition will be 10 .
So this analysis shows that any two binary digits can be added using the circuit. Remember that the circuit uses rules of binary addition, as follows -

```
0+0=0
0+1=1
1+0=1
1+1=10
```


### 1.18.1 FULL ADDER

It is also a combination of basic logic gates. It uses two half adder circuits connected one after another, as shown below. Using this circuit, we can add three binary digits at a time. In full adder, there are three inputs $A, B$ and $C$ with two outputs SUM and CARRY. The SUM and CARRY are the outputs. Remember that SUM is at LSB position and CARRY is at MSB position.

Here the outputs of first half adder are CARRY-1 and SUM-1. The output SUM-1 is connected to one input of next half adder. Its SUM output is taken as independent output. The CARRY-1 and CARRY-2 outputs of both half adders are $\boldsymbol{O R} \boldsymbol{e d}$ together to form a single CARRY output.

H.A.-2

The logic equations of the circuit are given below
CARRY1 $=A . B$
$S U M 1=A \oplus B$
CARRY2 $=(A \oplus B) \cdot C$
$S U M 2=A \oplus B \oplus C$
CARRY $=(A B)+(A \oplus B) \cdot C=A B+B C+A C$
$S U M=A \oplus B \oplus C$

| $\mathbf{A}$ | $\mathbf{B}$ | $\mathbf{C}$ | CARRY1 | SUM1 | CARRY2 | SUM2 | CARRY | SUM |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | $\mathbf{0}$ | $\mathbf{0}$ |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | $\mathbf{0}$ | $\mathbf{1}$ |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | $\mathbf{0}$ | $\mathbf{1}$ |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | $\mathbf{1}$ | $\mathbf{0}$ |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | $\mathbf{0}$ | $\mathbf{1}$ |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | $\mathbf{1}$ | $\mathbf{0}$ |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | $\mathbf{1}$ | $\mathbf{0}$ |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | $\mathbf{1}$ | $\mathbf{1}$ |

In this way, the outputs CARRY and SUM will become 11, only when all the inputs are 1 . And when only two inputs are 1 , then the outputs CARRY and SUM become 10.

### 1.19 THE 4-BIT BINARY ADDER

This circuit can add two 4-bit binary numbers. The process of addition in the circuit takes place as $A_{3} A_{2} A_{1} A_{0}+B_{3} B_{2} B_{1} B_{0}=S_{4} S_{3} S_{2} S_{1} S_{0}$. As shown in following figure, suppose $A_{3} A_{2} A_{1} A_{0}=1111$ and $B_{3} B_{2} B_{1} B_{0}=1111$, then we get the result of addition as $S_{4} S_{3} S_{2} S_{1} S_{0}=11110$ as follows -
$A_{0}=1$ and $B_{0}=1, \quad \therefore C_{0}=1$ and $S_{0}=0$.
$A_{1}=1$ and $B_{1}=1, \quad \therefore C_{1}=1$ and $S_{1}=1$.
$A_{2}=1$ and $B_{2}=1, \therefore C_{2}=1$ and $S_{2}=1$.
$A_{3}=1$ and $B_{3}=1, \quad \therefore C_{3}=S_{4}=1$ and $S_{3}=1$.
Finally, we get the output as $S_{4} S_{3} S_{2} S_{1} S_{0}=11110$.


### 1.20 CONTROLLED INVERTER USING EX-OR GATE

The Ex-OR gate can be used as controlled inverter circuit. So using four Ex-OR gates, four bit inverter circuit is shown in the following circuit diagram. When any one input terminal of Ex-OR gate is connected to logic-1, the gate works as NOT gate. Hence, Ex-OR gate can be used as controlled inverter. The circuit produces following results -


More examples of working of the circuit

| Control <br> input | Inputs <br> DCBA | Outputs <br> PQRS |
| :---: | :---: | :---: |
| 0 | 1101 | 1101 |
| 1 | 1101 | 0010 |
| 0 | 1000 | 1000 |
| 1 | 1000 | 0111 |

When $D C B A=1011$ and $C . I .=0$, then $P Q R S=1011$.
When $D C B A=1011$ and $C . I .=1$, then $P Q R S=0100$, which is the 1 's complement of 1011 .

When $D C B A=1111$ and $C . I .=0$, then $P Q R S=1111$.
When $D C B A=1111$ and $C . I .=1$, then $P Q R S=0000$, which is the 1 's complement of 1111 .
In this way the circuit produces the 1's complement of any number connected at its input when the value of C.I. $=1$. This circuit is very useful when we want to convert large binary number into its equivalent 1 's complement form.

### 1.21 ADDER/SUBTRACTOR LOGIC CIRCUIT

This circuit can perform both addition \& subtraction just by changing only one input known as "SUB" input. It is actually a combination of 4-bit adder circuit and controlled inverter circuit using Ex-OR gates. The four bit binary adder/subtractor circuit is given below -


Addition process: For addition keep $S U B=0$ and then connect two different binary numbers which we want to add. In this case, the circuit works as general-purpose binary adder circuit. All Ex-OR gates send the data at their outputs without any change, since the $S U B$ input is in logic 0 state. Thus, at output we get addition result as follows $A_{3} A_{2} A_{1} A_{0}+B_{3} B_{2} B_{1} B_{0}=S_{4} S_{3} S_{2} S_{1} S_{0}$.

Subtraction process: For subtraction keep $S U B=1$ and then connect two different binary numbers at two groups of inputs. The binary number which we want to subtract must be connected as $B_{3} B_{2} B_{1} B_{0}$ number. Now the circuit works as subtractor. The circuit performs subtraction process using 2 's complement method. The Ex-OR gates generate 1's complement of 'B' group number. Then this 1's complement is added to a 1 through $S U B=1$ at the input of rightmost full adder. Thus, at output we get subtraction result as follows -

$$
\begin{aligned}
& \quad \begin{array}{l}
\mathrm{A}_{3} \mathrm{~A}_{2} \mathrm{~A}_{1} \mathrm{~A}_{0} \\
\mathrm{D}_{3} \mathrm{D}_{2} \mathrm{D}_{1} \mathrm{D}_{0} \\
\frac{\mathrm{C}_{4} \mathrm{~S}_{3} \mathrm{~S}_{2} \mathrm{~S}_{1} \mathrm{~S}_{0}}{} \longleftarrow{ }^{\prime} \text { 's complement } \\
\text { of } \mathrm{B}_{3} \mathrm{~B}_{2} \mathrm{~B}_{1} \mathrm{~B}_{0}
\end{array} \\
& \mathrm{X} \longleftarrow \text { carry is ignored }
\end{aligned}
$$

## Objective questions

1. The output of $\qquad$ logic circuit becomes equal to logic-1 when both of its inputs are at logic-0.
2. When any one input of OR gate is at logic-1, its output is at $\qquad$ -.
3. When a NOT gate is connected at the input of an AND gate, the new gate produced is called as $\qquad$ .
4. In half adder circuit, when both of its inputs are logic-1, then its output is $\qquad$ and
$\qquad$ _.
5. When one input of 2-input Ex-OR gate is connected to logic-1, then the circuit behaves as $\qquad$ logic circuit.
6. According to De Morgan's theorem, $\overline{A+B+C}=$ $\qquad$ .
7. To construct an OR gate using NAND gates, as universal building block, the number of NAND gates required will be $\qquad$ .
8. When both inputs of an Ex-OR gate are at equal logic level, i.e. either at logic-1 or logic-0, then its output will be at $\qquad$ -
9. If two NOT gates are connected one after another, such that the output of first is connected to the input of second, and if initial input is at logic-0 level, then the final output will be at $\qquad$ -.
10. The addition process of logic values can be performed using $\qquad$ gate.
11. Bubbled OR gate is equivalent to $\qquad$ gate.
12. $C+1=$ $\qquad$ .

## Short answer questions (3 Marks)

1. Draw the symbol of NOT gate and explain its working with truth table.
2. Explain why NAND gate is known as universal building block?
3. How Ex-OR gate can be used as NOT gate? Explain.
4. How to convert a NOR gate into a NOT gate? Explain with diagram.
5. Prove that $C+A C+A B C+A B C D=C$
6. Explain the working of half adder using proper logic diagram.
7. What is parity? Explain the working of parity checker.
8. What is the basic difference between inclusive OR gate and exclusive OR gate? Explain with diagrams.

## Long answer questions (4 Marks)

1. Explain the working of NAND gate as universal building block by drawing different circuits as NOT, OR and AND gates.
2. How 4-bit binary adder circuit works? Explain with diagram and one example.
3. What is controlled inverter? How Exclusive OR gate can be used as controlled inverter? Explain with diagram.
4. Draw the circuit of 4-bit adder/subtractor circuit using full adders and the circuit of controlled inverter.
5. Define and prove De Morgan's both theorems with diagrams and truth tables.
6. Give any four logic equations to prove the Boolean algebra.
7. How full adder circuit works? Explain with diagram.
8. Explain the working of Ex-OR gate using basic gates. Draw the necessary diagram and explain the working of circuit with derivation of output equation.
9. How to use NAND gates to produce one exclusive OR gate? Explain with diagram and derivation of output equation.
10. Prove that NOR can gate be used as universal building block with diagram and derivations of each circuit.
11. Draw the logic circuit of 4-input Ex-OR gate and explain its working such that its output equation will be $Y=A \oplus B \oplus C \oplus D$.
12. Define and explain the three basic gates. Write their truth tables also.
13. Solve the following identities and prove that LHS = RHS.
$\overline{A B+B C+C A}=\bar{A} \cdot \bar{B}+\bar{B} \cdot \bar{C}+\bar{C} \cdot \bar{A}$
$\overline{\bar{A}+B}+\overline{\bar{A}+\bar{B}}=A$
$A B+C A B+D B C A+D B A C E=$
A. $(\bar{A}+B)=A B$

## Conceptual study questions



1. Is there an alternative to check the parities using some other logic circuit? Explain with reasons.
2. How you can produce 10 input Exclusive OR gate? Explain with diagram.
3. Can we replace controlled inverter circuit used in 4-bit binary adder with simple NOT logic circuit? Explain.
4. Try to solve the famous Boatman's puzzle by drawing its equivalent logic circuit and final output equation.

Notes Space

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